19-3142; Rev 5; 11/09

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

General Description

The single MAX4036/MAX4037 and dual MAX4038/MAX4039 operational amplifiers operate from a single +1.4V to +3.6V (without reference) or +1.8V to +3.6V (with reference) supply and consume only 800nA of supply current per amplifier, and 1.1µA for the optional reference. The MAX4036/MAX4038 feature a common-mode input voltage range from 0V to V_{DD} - 0.4V at V_{DD} = 1.4V. The MAX4037/MAX4039 feature a 1.232V voltage reference capable of sourcing 100µA and sinking 20µA.

The MAX4036–MAX4039s' rail-to-rail outputs drive 5kΩ loads to within 25mV of the rails. Ultra-low supply current, low operating voltage, and rail-to-rail outputs make the MAX4036–MAX4039 ideal for use in single-cell lithium-ion (Li+), or two-cell NiCd/NiMH/alkaline battery-powered applications.

The MAX4036 is available in an SC70 package, the MAX4037 in a SOT23 package, and the MAX4038/MAX4039 in UCSP™, µMAX®, and TDFN packages.

Applications

Battery-Powered/Solar-Powered Systems

Portable Medical Instrumentation

Pagers and Cell Phones

Micropower Thermostats and Potentiostats

Electrometer Amplifiers

Remote Sensor Amplifiers

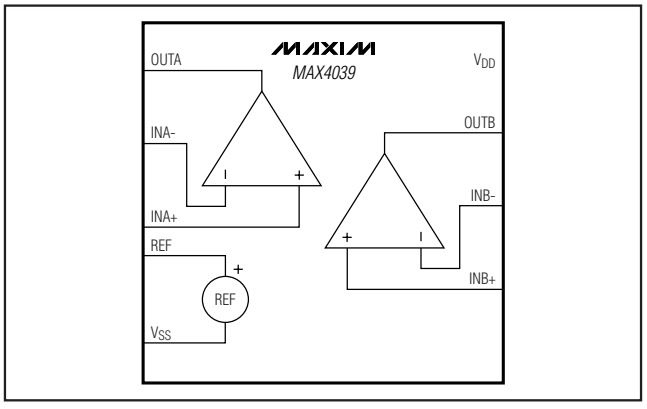
Active Badges

pH Meters

Pin Configurations and Selector Guide appear at end of data sheet.

µMAX is a registered trademark and UCSP is a trademark of Maxim Integrated Products, Inc.

Functional Diagram



Features

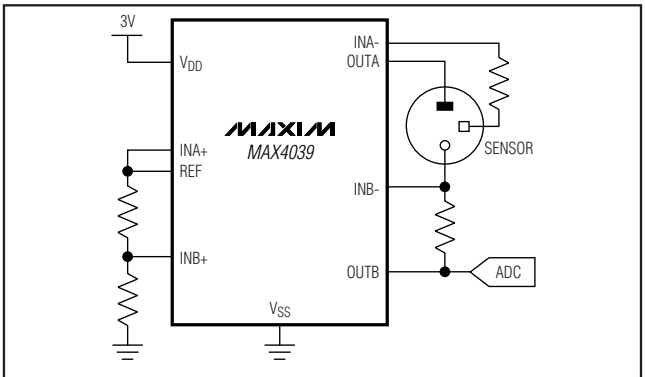
- **Ultra-Low 800nA per Amplifier Supply Current**
- **Ultra-Low 1.4V Supply Voltage Operation (1.8V for MAX4037/MAX4039)**
- **Rail-to-Rail Outputs Drive 5kΩ and 5000pF Load**
- **1.232V ±0.5%, 120ppm/°C (max) Reference (MAX4037/MAX4039)**
- **No External Reference Bypass Capacitor Required**
- **No Phase Reversal for Overdriven Inputs**
- **Low 1.0pA (typ) Input Bias Current**
- **Low 200µV Input Offset Voltage**
- **Unity-Gain Stable**
- **Available in Tiny UCSP, SC70, SOT23, TDFN, and µMAX Packages**
- **Available in -40°C to +125°C Temperature Range (MAX4036A/MAX4038A)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4036EXK-T	-40°C to +85°C	5 SC70	AFR
MAX4036AAXK+T	-40°C to +125°C	5 SC70	ASN
MAX4037EUT-T	-40°C to +85°C	6 SOT23	ABRX
MAX4038ETA-T	-40°C to +85°C	8 TDFN-EP*	AGO
MAX4038EUA	-40°C to +85°C	8 µMAX	—
MAX4038EBL-T	-40°C to +85°C	9 UCSP	AEG
MAX4038AAUA	-40°C to +125°C	8 µMAX	—

+Denotes a lead(Pb)-free/RoHS-compliant package.
-Denotes a package containing lead.
**EP = Exposed pad.*
Ordering Information continued at end of data sheet.

Typical Operating Circuit



THREE-ELECTRODE POTENTIOSTAT APPLICATION

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to V_{SS} .....-0.3V to +4.0V
INA+, INB+, INA-, INB-, IN+, IN-, OUTA, OUTB, OUT, REF .....(V_{SS} - 0.3V) to (V_{DD} + 0.3V)
OUTA, OUTB, OUT, REF Shorted to V_{SS} or V_{DD} .....Continuous
Maximum Continuous Power Dissipation (T_A = +70°C)
5-Pin SC70 (derate 3.1mW/°C above +70°C).....247mW
6-Pin SOT23 (derate 8.7mW/°C above +70°C).....696mW
8-Pin µMAX (derate 4.5mW/°C above +70°C).....362mW
8-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
9-Bump UCSP (derate 5.2mW/°C above +70°C).....412mW
10-Pin µMAX (derate 5.6mW/°C above +70°C).....444mW
10-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range
MAX403_E_ _.....-40°C to +85°C
MAX403_A_ _ .....-40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V, V_{SS} = V_{CM} = 0V, $V_{OUT_}$ = V_{DD}/2, R_L to V_{DD}/2, C_L = 15pF, **T_A = +25°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	MAX4036/MAX4038, guaranteed by PSRR tests		1.4		3.6	V
		MAX4037/MAX4039, guaranteed by PSRR and line regulation tests		1.8		3.6	
Supply Current	I_{DD}	MAX4036	V_{DD} = 1.4V		0.8	1.2	µA
			V_{DD} = 3.6V		0.9	1.3	
		MAX4037	V_{DD} = 1.8V		1.9	2.4	
			V_{DD} = 3.6V		2.0	2.5	
		MAX4038	V_{DD} = 1.4V		1.7	2.3	
			V_{DD} = 3.6V		1.9	2.5	
		MAX4039	V_{DD} = 1.8V		2.8	4.0	
			V_{DD} = 3.6V		3.0	4.1	
OPERATIONAL AMPLIFIERS							
Input Offset Voltage	V_{OS}				±0.2	±2.0	mV
Input Bias Current	I_B	(Note 1)			±1.0	±10	pA
Input Offset Current	I_{OS}	(Note 1)			±0.3	±20	pA
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR test	V_{DD} = 1.4V (MAX4036/MAX4038 only)	V_{SS}		V_{DD} - 0.4	V
			V_{DD} = 1.8V	V_{SS}		V_{DD} - 0.3	
			V_{DD} = 3.3V	V_{SS}		V_{DD} - 0.2	
Common-Mode Rejection Ratio	CMRR	V_{DD} = 1.4V, $V_{SS} \le V_{CM} \le (V_{DD}$ - 0.4V) (MAX4036/MAX4038 only)		50	70		dB
		V_{DD} = 1.8V, $V_{SS} \le V_{CM} \le (V_{DD}$ - 0.3V)		50	70		
		V_{DD} = 3.3V, $V_{SS} \le V_{CM} \le (V_{DD}$ - 0.2V)		56	76		
Power-Supply Rejection Ratio	PSRR	1.4V ≤ V_{DD} ≤ 3.6V (MAX4036/MAX4038 only)		62	82		dB
		1.8V ≤ V_{DD} ≤ 3.6V		62	84		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{SS} = V_{CM} = 0V, $V_{OUT_}$ = V_{DD}/2, R_L to V_{DD}/2, C_L = 15pF, **T_A = +25°C**, unless otherwise specified.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Large-Signal Voltage Gain	A_{VOL}	R_L = 100kΩ, 50mV ≤ V_{OUT} ≤ (V_{DD} - 50mV)	80	108		dB
		R_L = 5kΩ, 150mV ≤ V_{OUT} ≤ (V_{DD} - 150mV)	78	105		
Output Voltage Swing High	V_{DD} - V_{OH}	R_L = 100kΩ		2	5	mV
		R_L = 5kΩ		25	50	
Output Voltage Swing Low	V_{OL} - V_{SS}	R_L = 100kΩ		2	5	mV
		R_L = 5kΩ		25	50	
Output Short-Circuit Current	I_{SCO}	To V_{DD} or V_{SS}		±13		mA
Gain-Bandwidth Product	GBW			4		kHz
Phase Margin	θ_M			90		Degrees
Slew Rate	SR			4		V/ms
Power-On Time	t_{ON}	(Note 3)		0.25		ms
Input Noise-Voltage Density	e_n	f = 1kHz		500		nV/√Hz
Capacitive-Load Stability	C_{LOAD}	A_{VCL} = 1V/V, no sustained oscillations		5000		pF
REFERENCE (MAX4037/MAX4039)						
Reference Voltage	V_{REF}		1.226	1.232	1.238	V
Line Regulation	$\Delta V_{REF}/\Delta V_{DD}$	V_{DD} = +1.8V to +3.6V			0.3	%/V
Load Regulation	$\Delta V_{REF}/\Delta I_{LOAD}$	0 ≤ I_{LOAD} ≤ 100µA, sourcing			0.0015	%/µA
		-20µA ≤ I_{LOAD} ≤ 0, sinking			0.0075	
Reference Output Voltage Noise	e_n	0.1Hz to 10Hz		60		μV_{P-P}
Output Short-Circuit Current	I_{SCR}	Short to V_{DD}		0.25		mA
		Short to V_{SS}		1.9		
Capacitive-Load Stability Range	C_{LOAD}	(Note 1)	0		250	pF

ELECTRICAL CHARACTERISTICS

(V_{DD} = +3V, V_{SS} = V_{CM} = 0V, $V_{OUT_}$ = V_{DD}/2, R_L to V_{DD}/2, C_L = 15pF, **T_A = T_{MIN} to T_{MAX}**, unless otherwise specified.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	MAX4036/MAX4038, guaranteed by PSRR test		1.4		3.6	V
		MAX4037/MAX4039, guaranteed by PSRR and line regulation tests		1.8		3.6	
Supply Current	I_{DD}	MAX4036	V_{DD} = 1.4V			1.7	µA
			V_{DD} = 3.6V			1.8	
		MAX4036A	V_{DD} = 1.4V			2.0	
			V_{DD} = 3.6V			2.1	
		MAX4037	V_{DD} = 1.8V			3.1	
			V_{DD} = 3.6V			3.2	

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +3V, V_{SS} = V_{CM} = 0V, $V_{OUT_}$ = V_{DD}/2, R_L to V_{DD}/2, C_L = 15pF, **T_A = T_{MIN} to T_{MAX}**, unless otherwise specified.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{DD}	MAX4038	V_{DD} = 1.4V			2.9	µA
			V_{DD} = 3.6V			3.2	
		MAX4038A	V_{DD} = 1.4V			3.4	
			V_{DD} = 3.6V			3.7	
		MAX4039	V_{DD} = 1.8V			5.2	
			V_{DD} = 3.6V			5.3	
OPERATIONAL AMPLIFIERS							
Input Offset Voltage	V_{OS}					±8	mV
Input Offset Voltage Temperature Coefficient	TCV_{OS}				±1		µV/°C
Input Bias Current	I_B					±100	pA
Input Offset Current	I_{OS}					±200	pA
Input Common-Mode Voltage Range	V_{CM}	Guaranteed by CMRR test	V_{DD} = 1.4V (MAX4036/MAX4038 only)	V_{SS}		V_{DD} - 0.4	V
			V_{DD} = 1.8V	V_{SS}		V_{DD} - 0.4	
			V_{DD} = 3.3V	V_{SS}		V_{DD} - 0.2	
Common-Mode Rejection Ratio	CMRR	V_{DD} = 1.4V, $V_{SS} \le V_{CM} \le (V_{DD}$ - 0.5V) (MAX4036/MAX4038 only)		44			dB
		V_{DD} = 1.8V, $V_{SS} \le V_{CM} \le (V_{DD}$ - 0.4V)		50			
		V_{DD} = 3.3V, $V_{SS} \le V_{CM} \le (V_{DD}$ - 0.3V)		52			
Power-Supply Rejection Ratio	PSRR	1.4V ≤ V_{DD} ≤ 3.6V (MAX4036/MAX4038 only)		60			dB
		1.8V ≤ V_{DD} ≤ 3.6V		60			
Large-Signal Voltage Gain	A_{VOL}	R_L = 100kΩ, 50mV ≤ $V_{OUT} \le (V_{DD}$ - 50mV)		75			dB
		R_L = 5kΩ, 150mV ≤ $V_{OUT} \le (V_{DD}$ - 150mV)		73			
Output Voltage Swing High	V_{DD} - V_{OH}	R_L = 100kΩ				10	mV
		R_L = 5kΩ				100	
Output Voltage Swing Low	V_{OL} - V_{SS}	R_L = 100kΩ				10	mV
		R_L = 5kΩ				100	
REFERENCE (MAX4037/MAX4039)							
Reference Voltage Temperature Coefficient	TCV_{REF}	(Note 1)	MAX4037EUT-T, MAX4039ETB, MAX4039EUB		25	120	ppm/°C
			MAX4039EBL-T		35	200	
Line Regulation	$\Delta V_{REF}/\Delta V_{DD}$	V_{DD} = 1.8V to 3.6V				0.6	%/V
Load Regulation	$\Delta V_{REF}/\Delta I_{LOAD}$	0 ≤ I_{LOAD} ≤ 100µA, sourcing				0.003	%/µA
		-20µA ≤ I_{LOAD} ≤ 0, sinking				0.015	
Capacitive-Load Stability Range	C_{LOAD}	(Note 1)		0		250	pF

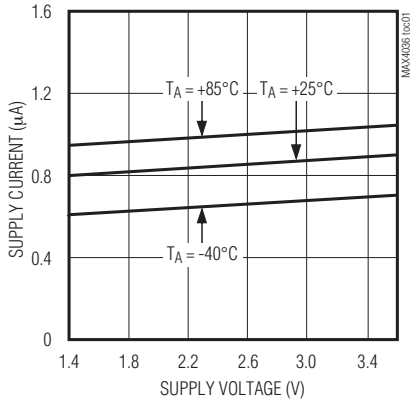
Note 1: Guaranteed by design.
Note 2: All devices are production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 3: Output settles within 1% of final value.

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

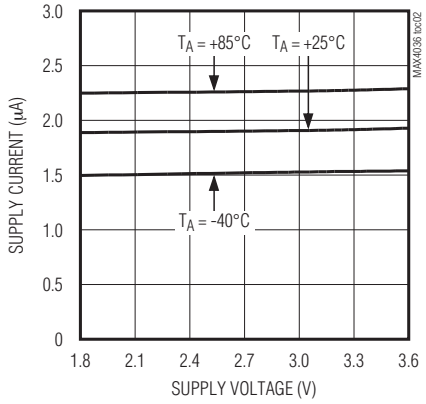
Typical Operating Characteristics

(V_{DD} = 3V, V_{SS} = V_{CM} = 0V, R_L to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

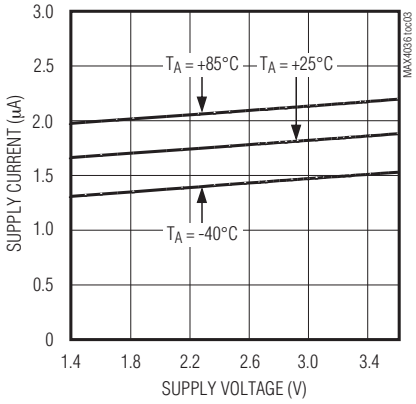
MAX4036
SUPPLY CURRENT
vs. SUPPLY VOLTAGE AND TEMPERATURE



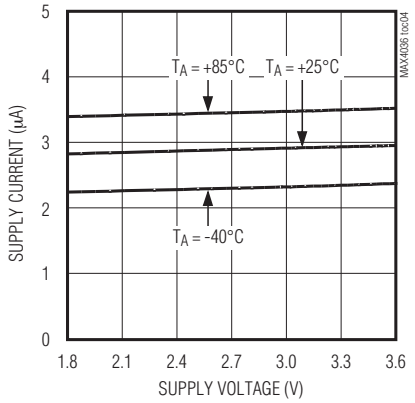
MAX4037
SUPPLY CURRENT
vs. SUPPLY VOLTAGE AND TEMPERATURE



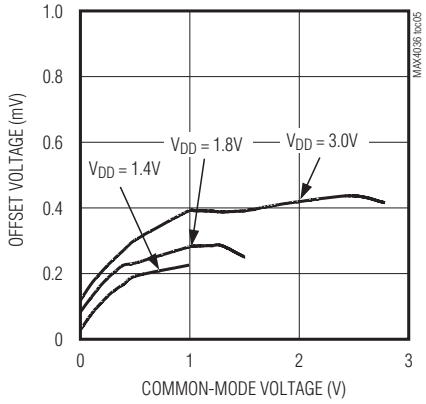
MAX4038
SUPPLY CURRENT
vs. SUPPLY VOLTAGE AND TEMPERATURE



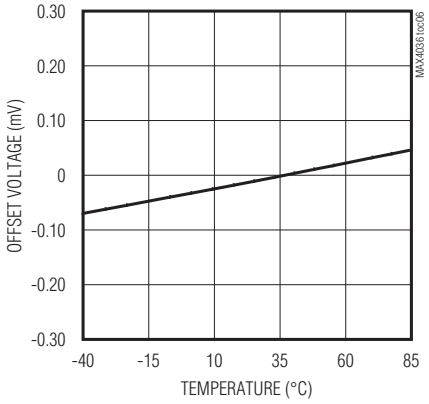
MAX4039
SUPPLY CURRENT
vs. SUPPLY VOLTAGE AND TEMPERATURE



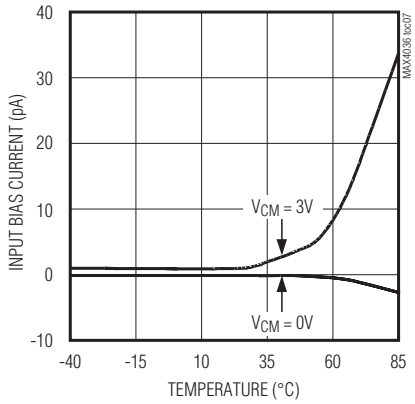
OFFSET VOLTAGE
vs. COMMON-MODE VOLTAGE



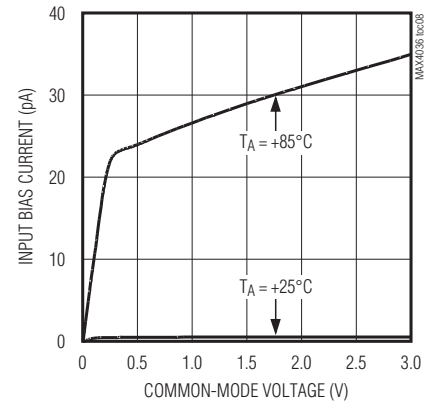
OFFSET VOLTAGE
vs. TEMPERATURE



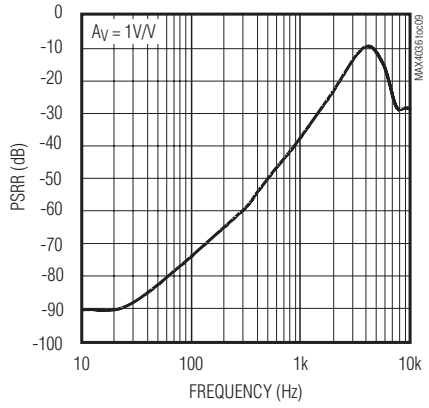
INPUT BIAS CURRENT
vs. TEMPERATURE



INPUT BIAS CURRENT
vs. COMMON-MODE VOLTAGE



OP AMP POWER-SUPPLY REJECTION RATIO
vs. FREQUENCY

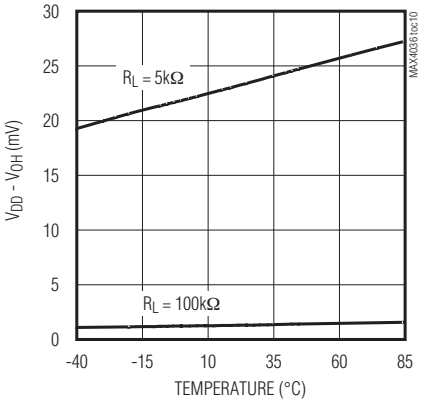


Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

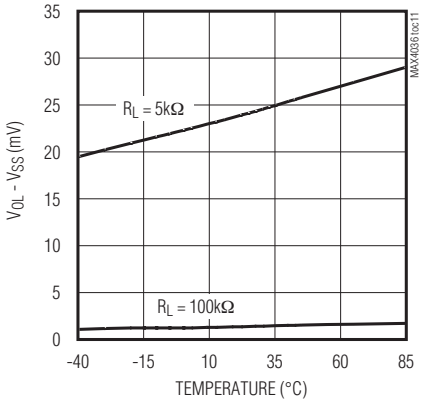
Typical Operating Characteristics (continued)

(V_{DD} = 3V, V_{SS} = V_{CM} = 0V, R_L to $V_{DD}/2$, T_A = +25°C, unless otherwise noted.)

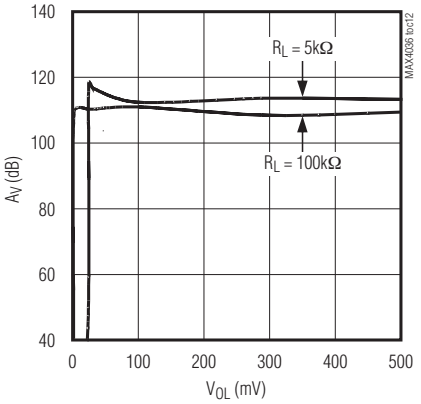
OUTPUT VOLTAGE SWING HIGH vs. TEMPERATURE



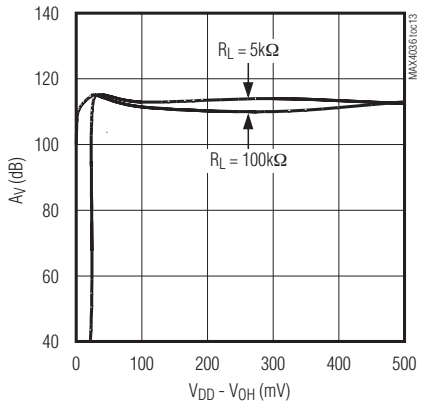
OUTPUT VOLTAGE SWING LOW vs. TEMPERATURE



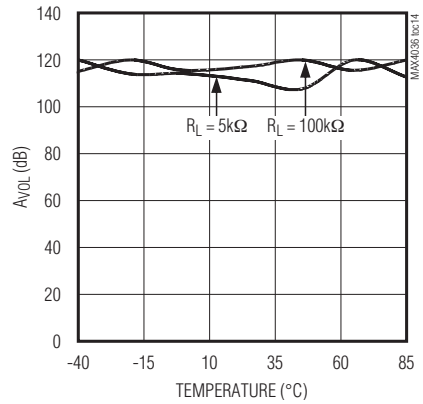
AV vs. OUTPUT SWING LOW



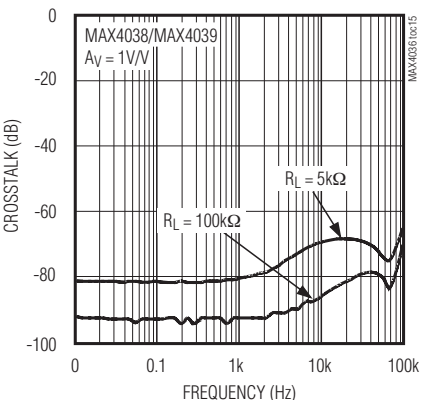
AV vs. OUTPUT SWING HIGH



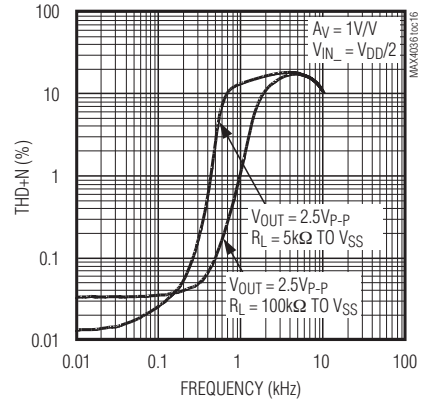
AV vs. TEMPERATURE



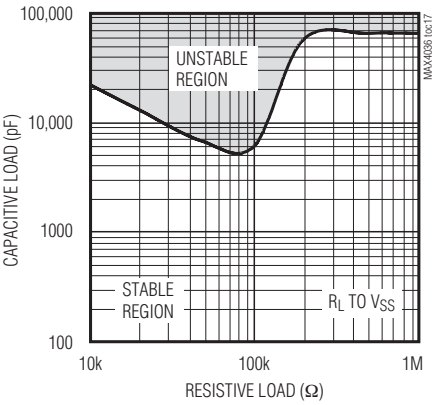
CROSSTALK vs. FREQUENCY



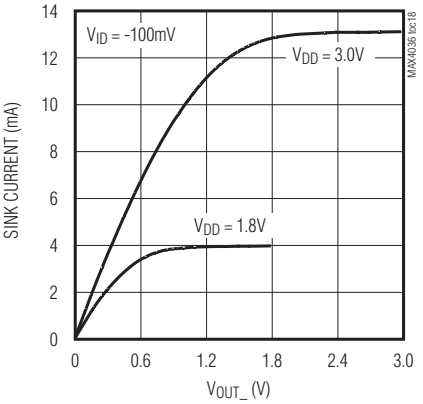
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



OP AMP STABILITY vs. CAPACITIVE AND RESISTIVE LOADS



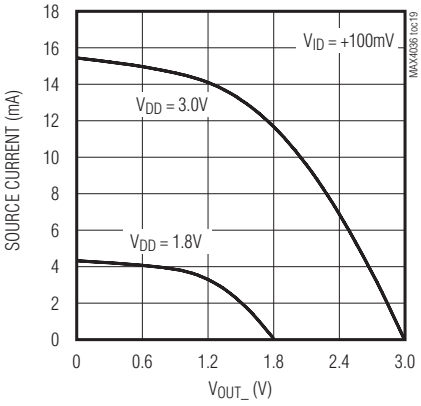
OP AMP SINK CURRENT vs. OUTPUT VOLTAGE



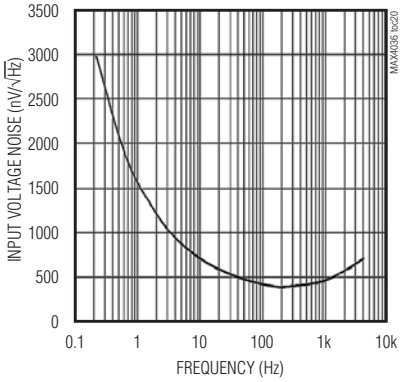
Typical Operating Characteristics (continued)

(V_{DD} = 3V, V_{SS} = V_{CM} = 0V, R_L to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

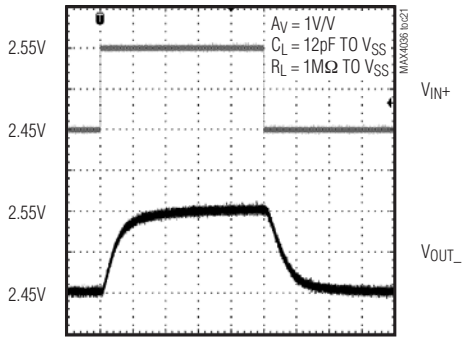
OP AMP SOURCE CURRENT vs. OUTPUT VOLTAGE



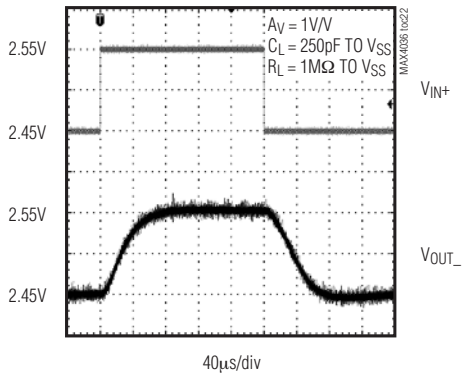
INPUT VOLTAGE NOISE DENSITY vs. FREQUENCY



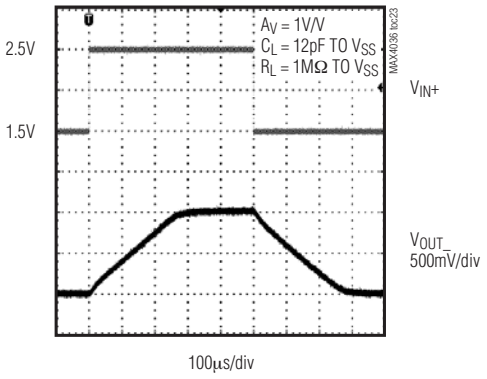
OP AMP SMALL-SIGNAL TRANSIENT RESPONSE



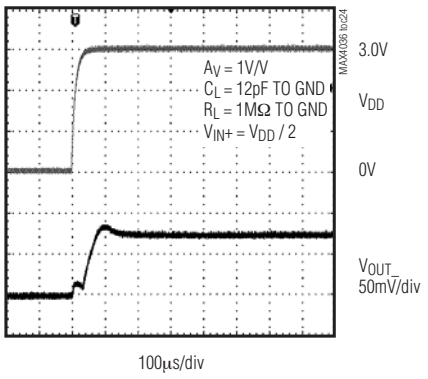
OP AMP SMALL-SIGNAL TRANSIENT RESPONSE



OP AMP LARGE-SIGNAL TRANSIENT RESPONSE



OP AMP TURN-ON TRANSIENT RESPONSE

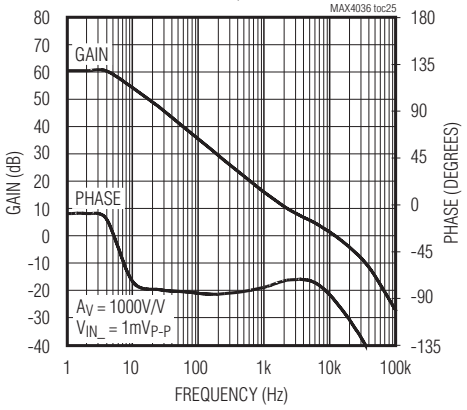


Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

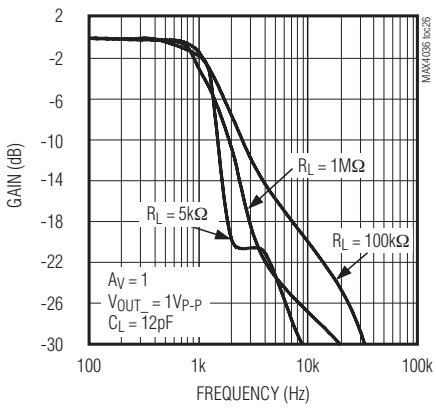
Typical Operating Characteristics (continued)

(V_{DD} = 3V, V_{SS} = V_{CM} = 0V, R_L to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

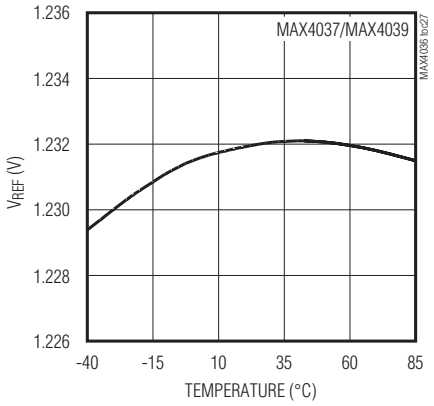
GAIN AND PHASE vs. FREQUENCY



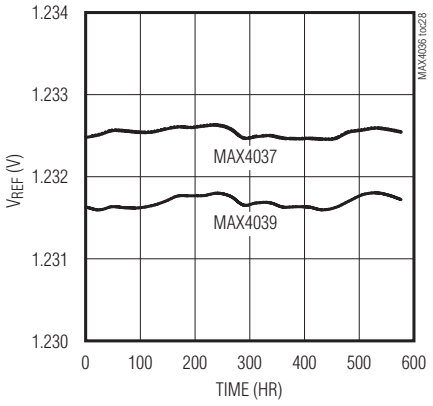
LARGE-SIGNAL GAIN vs. FREQUENCY



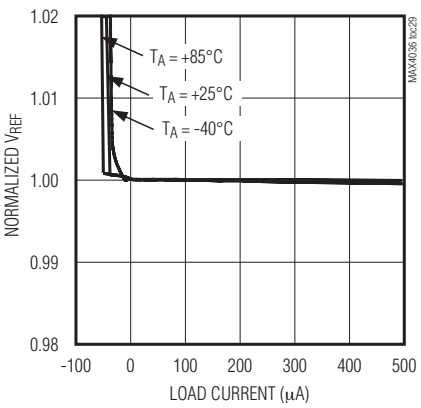
REFERENCE VOLTAGE vs. TEMPERATURE



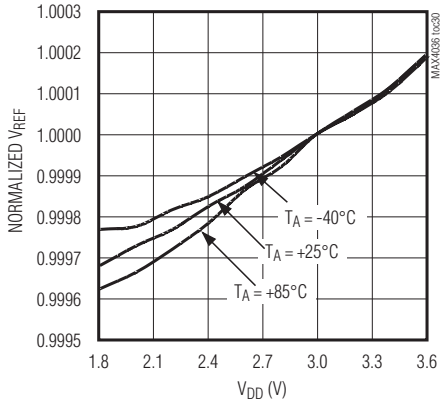
REFERENCE VOLTAGE CHANGE vs. TIME



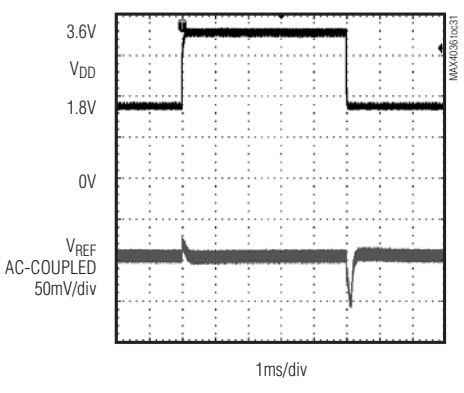
REFERENCE VOLTAGE CHANGE vs. LOAD CURRENT



REFERENCE VOLTAGE CHANGE vs. SUPPLY VOLTAGE



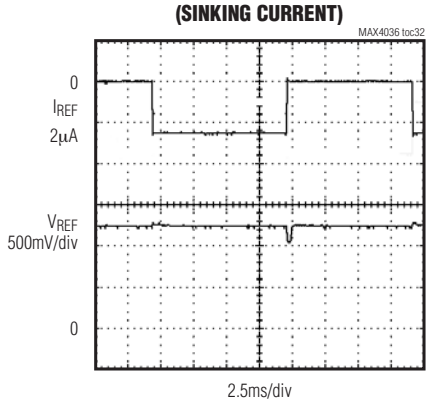
REFERENCE LINE-TRANSIENT RESPONSE



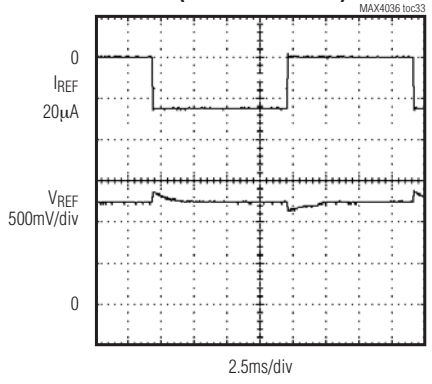
Typical Operating Characteristics (continued)

(V_{DD} = 3V, V_{SS} = V_{CM} = 0V, R_L to V_{DD}/2, T_A = +25°C, unless otherwise noted.)

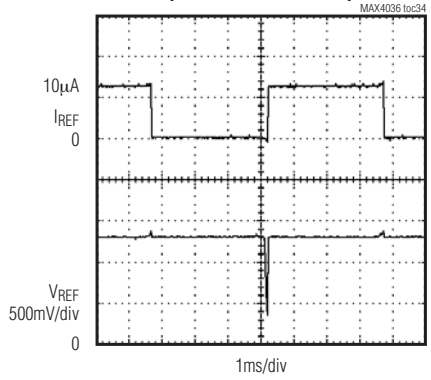
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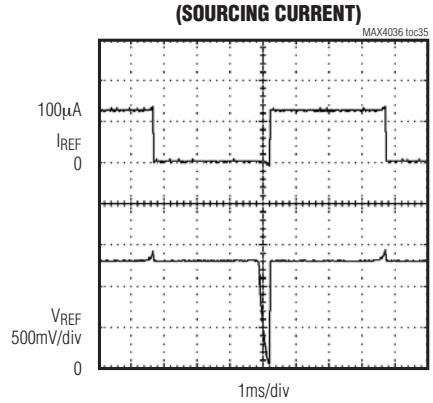
REFERENCE LOAD-TRANSIENT RESPONSE (SINKING CURRENT)



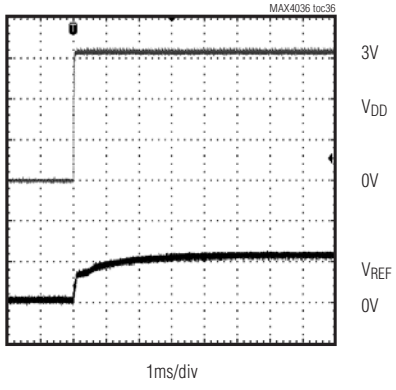
REFERENCE LOAD-TRANSIENT RESPONSE (SOURCING CURRENT)



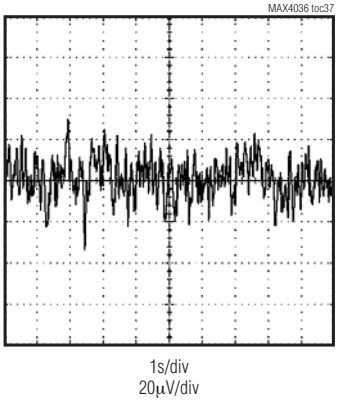
REFERENCE LOAD-TRANSIENT RESPONSE (SOURCING CURRENT)



REFERENCE TURN-ON TRANSIENT RESPONSE



0.1Hz TO 10Hz REFERENCE NOISE



Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

PIN						NAME	FUNCTION
MAX4036/ MAX4036A	MAX4037	MAX4038/ MAX4038A		MAX4039			
		µMAX*/TDFN	UCSP	µMAX/TDF	UCSP		
1	3	—	—	—	—	IN+	Noninverting Amplifier Input
2	2	4	A2	5	A2	V_{SS}	Negative Power-Supply Voltage
3	4	—	—	—	—	IN-	Inverting Amplifier Input
4	1	—	—	—	—	OUT	Amplifier Output
5	6	8	C2	10	C2	V_{DD}	Positive Power-Supply Voltage
—	5	—	—	6	B2	REF	Reference Voltage Output
—	—	1	C1	1	C1	OUTA	Amplifier Output (Channel A)
—	—	2	B1	2	B1	INA-	Inverting Amplifier Input (Channel A)
—	—	3	A1	3	A1	INA+	Noninverting Amplifier Input (Channel A)
—	—	5	A3	7	A3	INB+	Noninverting Amplifier Input (Channel B)
—	—	6	B3	8	B3	INB-	Inverting Amplifier Input (Channel B)
—	—	7	C3	9	C3	OUTB	Amplifier Output (Channel B)
—	—	—	B2	4	—	N.C.	No Connection. Not internally connected.
—	—	—	—	—	—	EP (TDFN only)	Exposed Paddle. Solder EP to V_{SS} or leave unconnected (TDFN packages only).

**Both MAX4038/MAX4038A available in µMAX package only.*

Detailed Description

The MAX4036–MAX4039 consume an ultra-low supply current and have rail-to-rail output stages specifically designed for low-voltage operation. The input common-mode voltage range extends from V_{DD} - 0.4V to V_{SS}, although full rail-to-rail input range is possible with degraded performance when operating from a supply voltage above 3.0V. The input offset voltage is typically 200µV. Low-operating supply voltage, low supply current, and rail-to-rail outputs make the MAX4036–MAX4039 an excellent choice for precision or general-purpose low-voltage, battery-powered systems.

Rail-to-Rail Outputs

The MAX4036–MAX4039 output stages can drive a 5kΩ load and still swing to within 40mV of the rails. Figure 1 shows the output voltage swing of the MAX4036–MAX4039 configured as a unity-gain buffer, powered from a single 2.4V supply. The output for this setup typically swings from 5mV to V_{DD} - 5mV with a 100kΩ load.

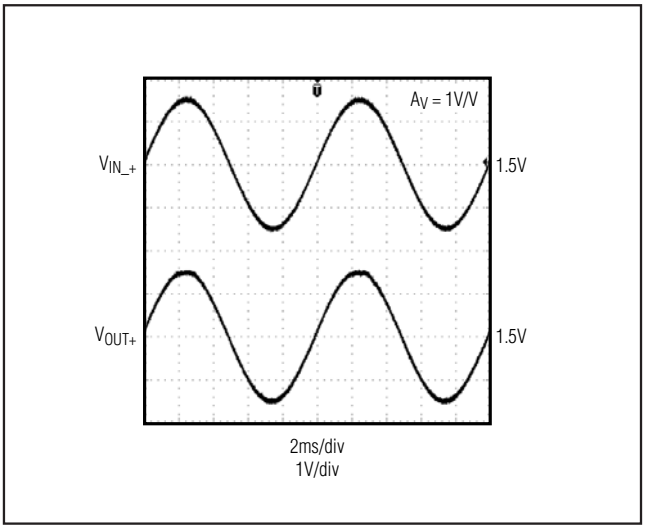


Figure 1. Rail-to-Rail Input/Output Voltage Range

Applications Information

Power-Supply Considerations

The MAX4036–MAX4039 operate from a single 1.4V (MAX4036/MAX4038) or 1.8V (MAX4037/MAX4039) to 3.6V supply. A high amplifier power-supply rejection ratio of 82dB and the excellent reference line regulation allow the devices to be powered directly from a decaying battery voltage, simplifying design and extending battery life. The MAX4036–MAX4039 are ideally suited for low-voltage battery-powered systems. The *Typical Operating Characteristics* show the changes in supply current and reference output as a function of supply voltage.

Power-Up Settling Time

The MAX4036–MAX4039 typically require 0.25ms to power-up. During this startup time, the output is indeterminate. The application circuit should allow for this initial delay. See the *Typical Operating Characteristics* for amplifier and reference settling time curves.

Driving Capacitive Loads: Op Amps

The MAX4036–MAX4039 amplifier(s) require no output capacitor for stability, and are unity-gain stable for loads up to 5000pF. Applications that require greater capacitive-drive capability should use an isolation resistor between the output and the capacitive load (Figure 2). Note that this solution reduces the gain and output voltage swing because R_{ISO} forms a voltage-divider with the load resistor.

Crossover Distortion

The MAX4036–MAX4039 output stages are capable of sourcing and sinking currents with orders of magnitude greater than the stages' quiescent current, which is less than 1µA. This ability to drive heavy loads with such a small quiescent current introduces crossover distortion as the output stage passes between sinking and sourcing. In the crossover regions, the output impedance of the MAX4036–MAX4039 increases substantially, thereby changing the load-driving characteristics. The distortion can be greatly reduced by increasing the load resistance. For applications where low load resistance is required, bias the load such that the output current is always in one direction, to avoid crossover distortion.

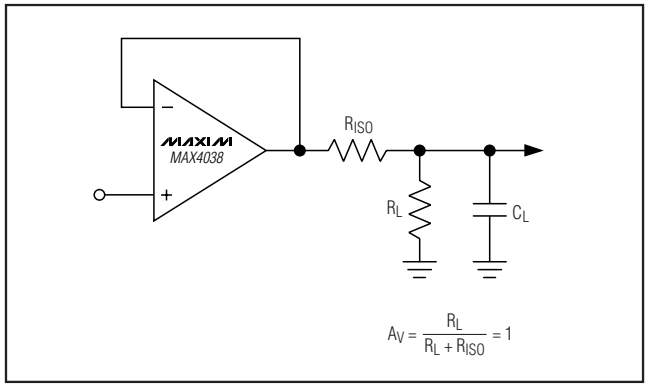


Figure 2. Using a Resistor to Isolate a Capacitive Load from the Op Amp

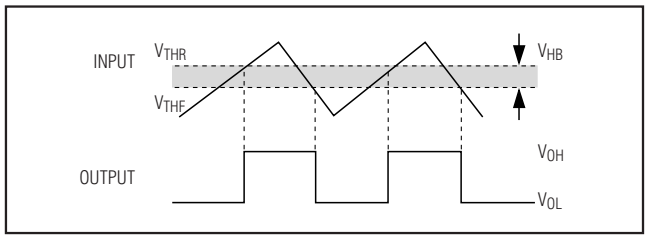


Figure 3. Hysteresis

Reference Bypassing

The MAX4037/MAX4039 reference requires no external capacitors.

Using the MAX4036–MAX4039 as a Comparator

Although optimized for use as an operational amplifier, the MAX4036–MAX4039 can be used as a rail-to-rail I/O comparator (Figures 3, 4). External hysteresis can be used to minimize the risk of output oscillation. The positive feedback circuit, shown in Figure 4, causes the input threshold to change when the output voltage changes state.

Battery Monitoring Using the MAX4037/MAX4039 and Hysteresis

The internal reference and low operating voltage of the MAX4037/MAX4039 make the devices ideal for battery-monitoring applications. Hysteresis can be set using resistors as shown in Figure 4, and the following design procedure:

1) Choose R3. The input bias current of IN_+ is under 100pA over temperature, so a current through R3 around 100nA maintains accuracy. The current through R3 at the trip point is V_{REF} / R3, or 100nA for R3 = 12MΩ. 10MΩ is a good practical value.

2) Choose the hysteresis voltage (V_{HB}), the voltage between the upper and lower thresholds. In this example, choose V_{HB} = 50mV (see Figure 3).

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

3) Calculate R1:

$$R1 = R3 \times \frac{V_{HB}}{V_{DD}}$$
$$= 10M\Omega \times \frac{0.5V}{2.4V}$$
$$= 210k\Omega$$

4) Choose the threshold voltage for V_{IN} rising (V_{THR}). In this example, choose V_{THR} = 2.0V.

5) Calculate R2:

$$R2 = \frac{1}{\left[\left(\frac{V_{THR}}{V_{REF} \times R1}\right) - \frac{1}{R1} - \frac{1}{R3}\right]}$$
$$= \frac{1}{\left[\left(\frac{2.0V}{1.2V \times 210k\Omega}\right) - \frac{1}{210k\Omega} - \frac{1}{10M\Omega}\right]}$$
$$= 325k\Omega$$

6) Verify the threshold voltages with these formulas:

V_{IN} rising:

$$V_{THR} = V_{REF} \times R1 \times \left(\frac{1}{R1} + \frac{1}{R2} + \frac{1}{R3}\right)$$

V_{IN} falling:

$$V_{THF} = V_{THR} - \left(\frac{R1 \times V_{DD}}{R3}\right)$$

In this application, the MAX4036–MAX4039 supply current will vary, depending on the output state of the comparator.

Power Supplies and Layout

The MAX4036–MAX4039 operate from a single 1.4V (MAX4036/MAX4038) or 1.8V (MAX4037/MAX4039) to 3.6V power supply. Bypass V_{DD} with a 0.1µF capacitor to ground to minimize noise.

Good layout techniques optimize performance by decreasing the amount of stray capacitance to the op amp's inputs and outputs. To decrease stray capacitance, minimize trace lengths by placing external components close to the device.

The exposed paddle (EP) on the TDFN packages of the MAX4038 and MAX4039 is internally connected to the device substrate, V_{SS}. Connect the exposed paddle to V_{SS} or leave EP unconnected. Running traces below the exposed paddle is not recommended.

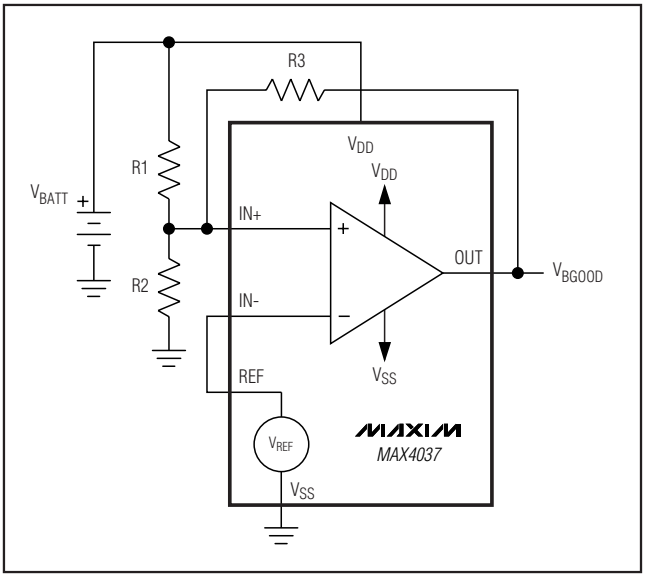


Figure 4. Battery Monitoring

Selector Guide

PART	NO. OF AMPLIFIERS	REFERENCE
MAX4036	1	—
MAX4037	1	√
MAX4038	2	—
MAX4039	2	√

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX4039EBL-T	-40°C to +85°C	9 UCSP	AEH
MAX4039ETB-T	-40°C to +85°C	10 TDFN-EP*	AAN
MAX4039EUB	-40°C to +85°C	10 µMAX	—

-Denotes a package containing lead.
**EP = Exposed pad.*

Chip Information

MAX4036 TRANSISTOR COUNT: 49

MAX4037 TRANSISTOR COUNT: 119

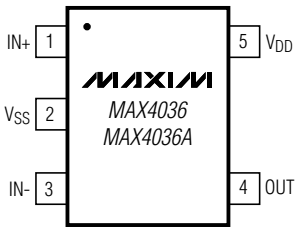
MAX4038 TRANSISTOR COUNT: 146

MAX4039 TRANSISTOR COUNT: 146

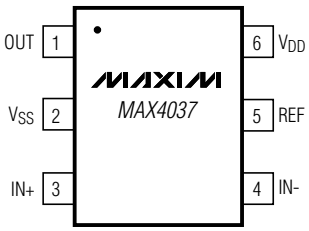
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Pin Configurations

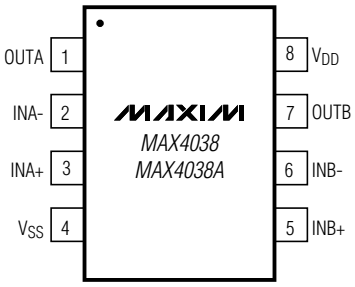
TOP VIEW



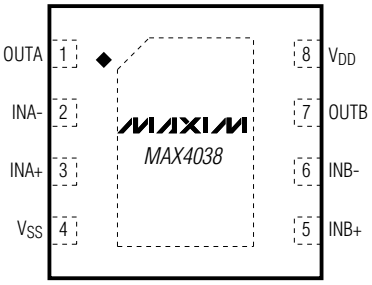
SC70



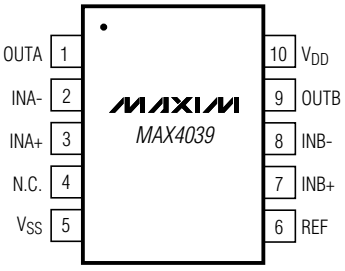
SOT23



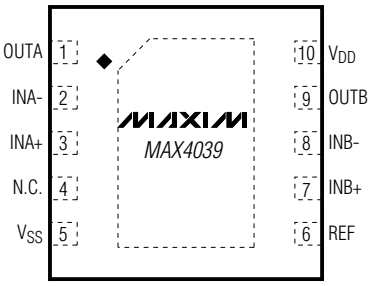
µMAX



3mm x 3mm x 0.8mm TDFN
TDFN EXPOSED PAD CONNECTED TO V_{SS}.



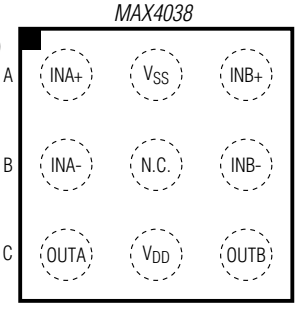
µMAX



3mm x 3mm x 0.8mm TDFN
TDFN EXPOSED PAD CONNECTED TO V_{SS}.

MAX4038

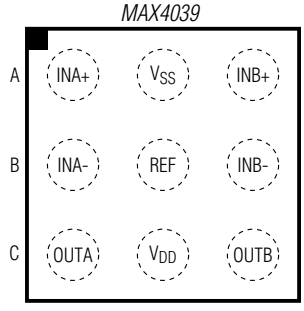
(BUMP SIDE DOWN)



UCSP

MAX4039

(BUMP SIDE DOWN)



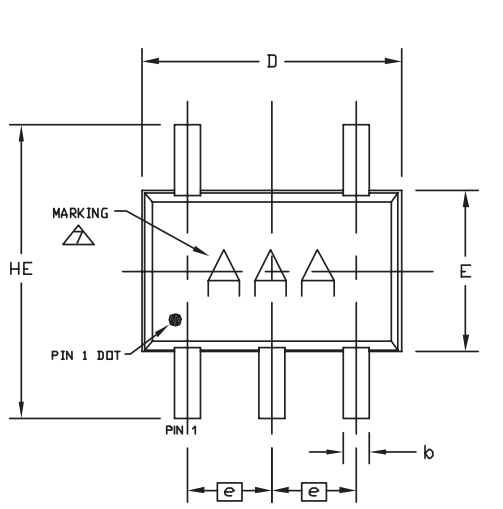
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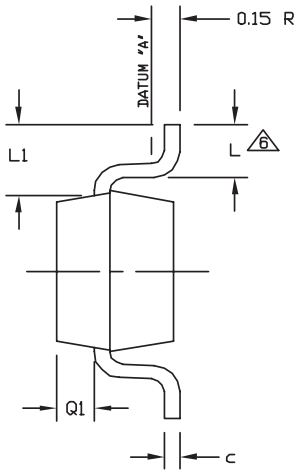
Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Package Information

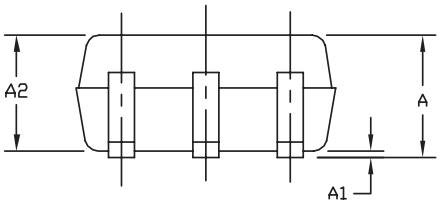
For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

SC70, 5L.EPS





COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.80	2.00	2.20
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.20	2.40
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODE	X5-1		



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COMPLY TO JEITA SC-88A EXCEPT FOR DIMENSION "L", ALL DIMENSIONS COMPLY TO JEDEC MO-203.
5. COPLANARITY 4 MILS. MAX.
6. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM "A" AND LEAD SURFACE.
7. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.

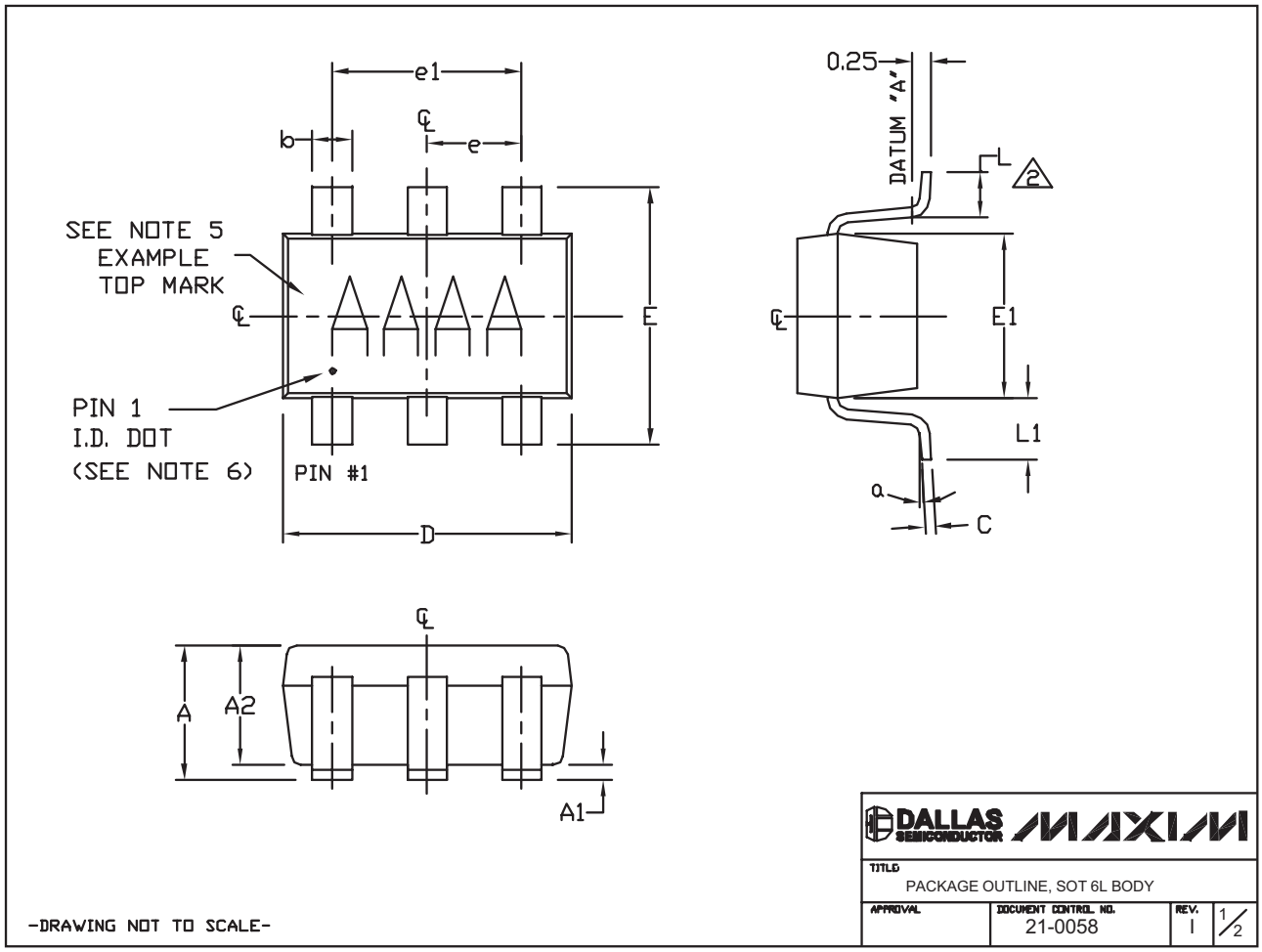
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DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 5L SC70			
APPROVAL	DOCUMENT CONTROL NO. 21-0076	REV. E	1/1

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

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NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25mm.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT. (SEE EXAMPLE TOP MARK)
6. PIN 1 I.D. DOT IS 0.3mm ø MIN. LOCATED ABOVE PIN 1.
7. MEETS JEDEC MO178, VARIATION AB.
8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.
9. LEAD TO BE COPLANAR WITHIN 0.1mm.
10. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

SYMBOL	MIN	NOMINAL	MAX
A	0.90	1.25	1.45
A1	0.00	0.05	0.15
A2	0.90	1.10	1.30
b	0.35	0.40	0.50
C	0.08	0.15	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.625	1.75
L	0.35	0.45	0.60
L1		0.60 REF.	
e1		1.90 BSC.	
e		0.95 BSC.	
α	0°	2.5°	10°

PKG CODES:
U6-1, U6-2, U6-4, U6C-8,
U6SN-1, U6CN-2, U6S-3, U6F-5,
U6F-6, U6FH-5, U6FH-6

-DRAWING NOT TO SCALE-

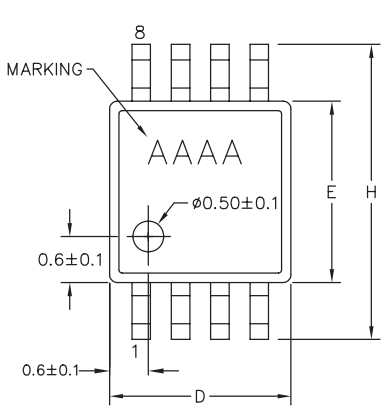
DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, SOT 6L BODY

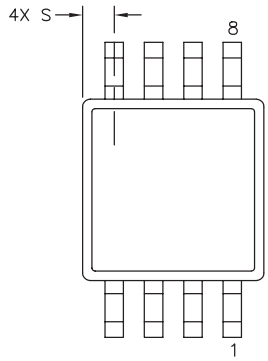
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0058	I	2/2

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



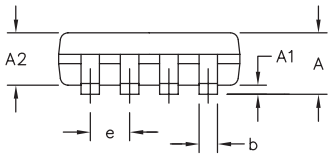
TOP VIEW



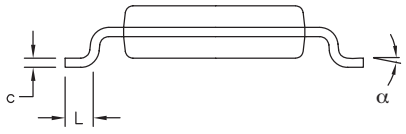
BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
b	0.010	0.014	0.25	0.36
c	0.005	0.007	0.13	0.18
D	0.114	0.122	2.90	3.10
e	0.0256 BSC		0.65 BSC	
E	0.114	0.122	2.90	3.10
H	0.188	0.198	4.78	5.03
L	0.016	0.026	0.41	0.66
α	0°	6°	0°	6°
S	0.0207 BSC		0.5250 BSC	

PKG. CODES:
U8–1; U8–3; U8CN–1



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15MM (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. COMPLIES TO JEDEC MO–187, LATEST REVISION, VARIATION AA.
5. MARKING SHOWN IS FOR PKG. ORIENTATION ONLY.
6. ALL DIMENSIONS APPLY TO BOTH LEADED (–) AND PbFREE (+) PKG. CODES.

–DRAWING NOT TO SCALE–

MAXIM

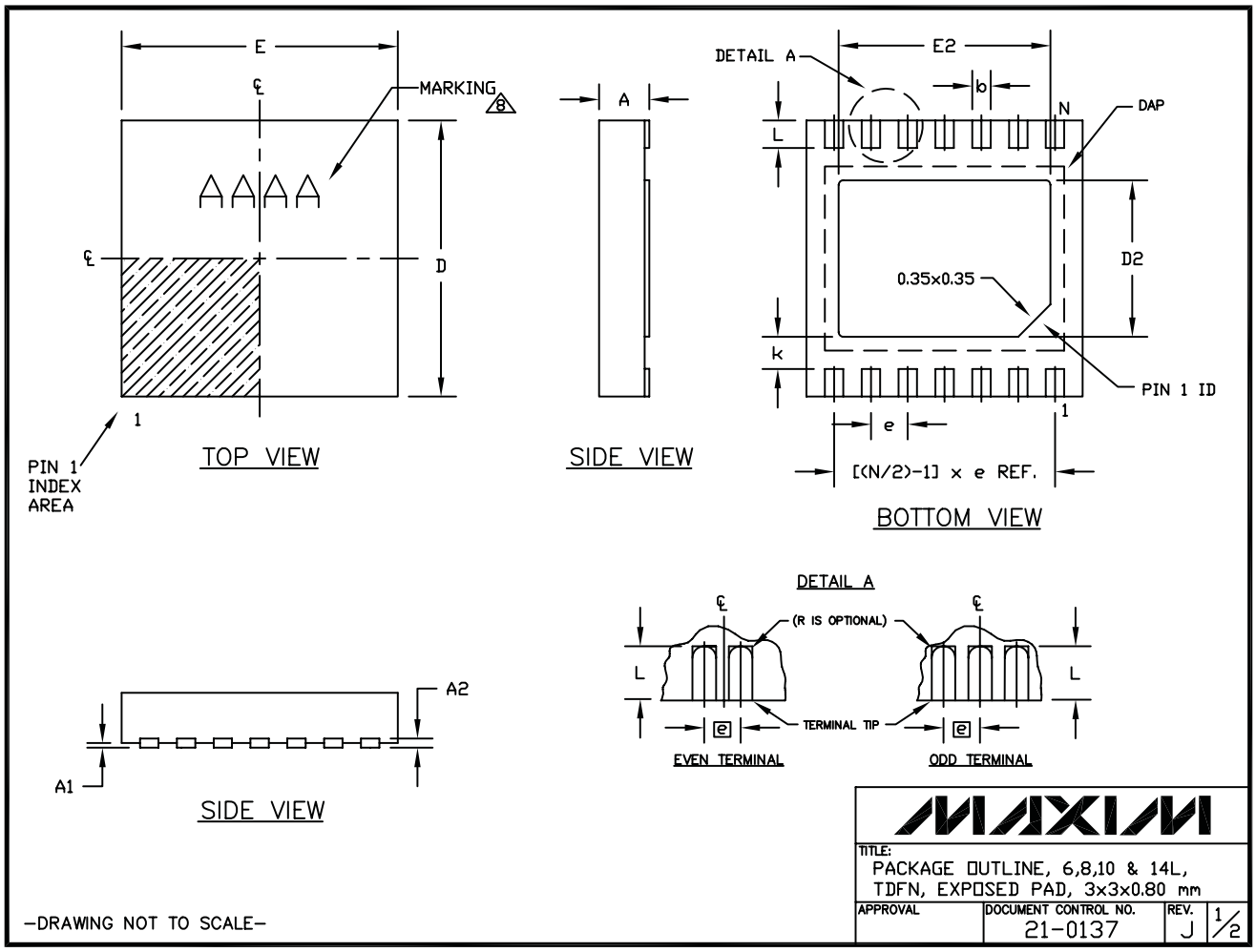
TITLE:
PACKAGE OUTLINE, 8L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21–0036	L	1/1

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033MK-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-3F	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

-DRAWING NOT TO SCALE-

MAXIM

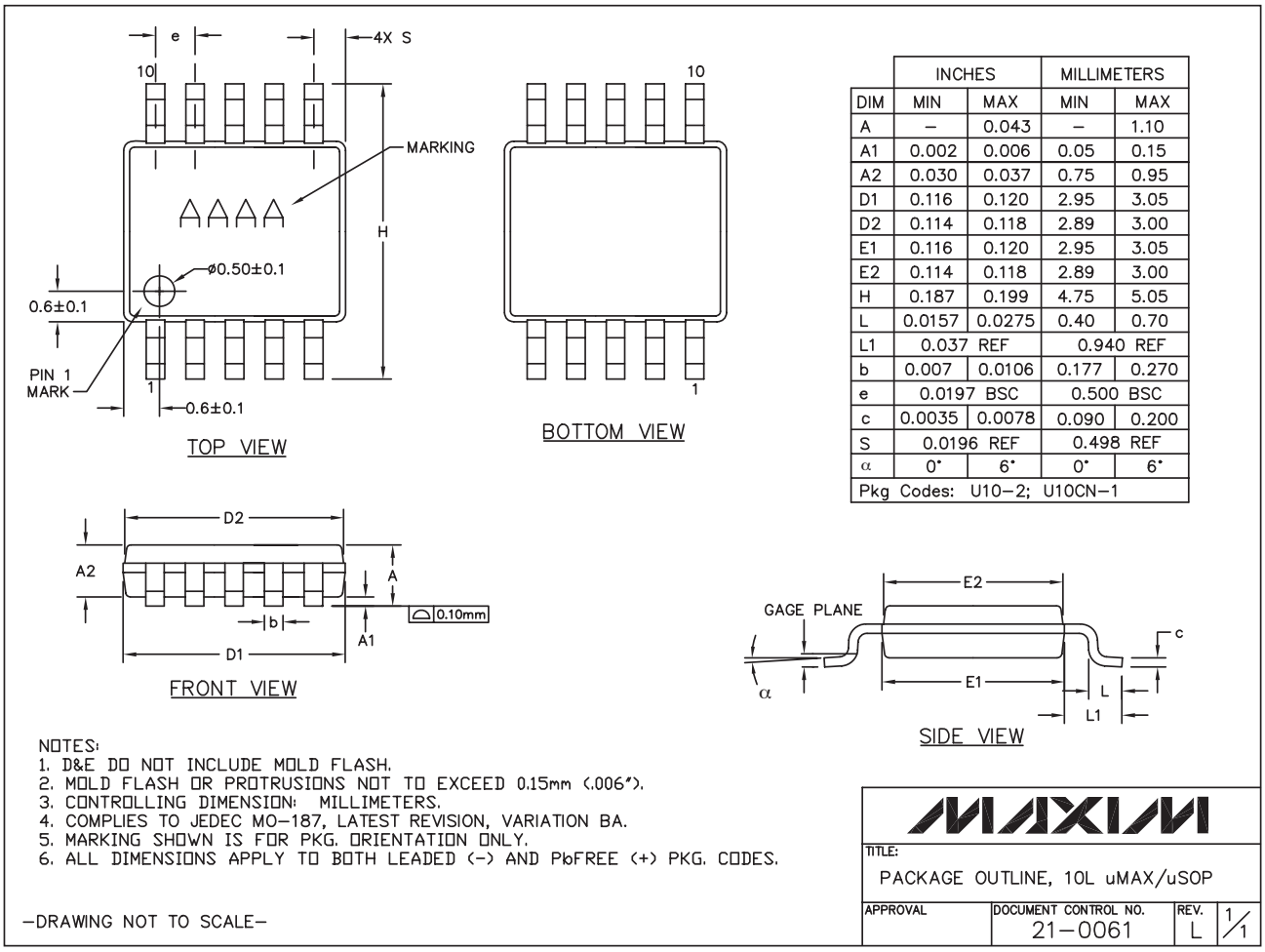
TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0137	J	2/2

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

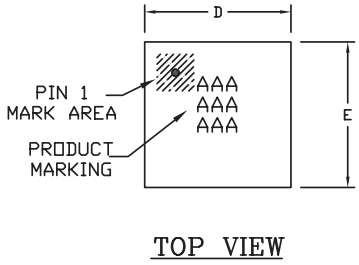


	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	–	0.043	–	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°
Pkg Codes: U10-2; U10CN-1				

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

9LUCSP, 3x3.EPS

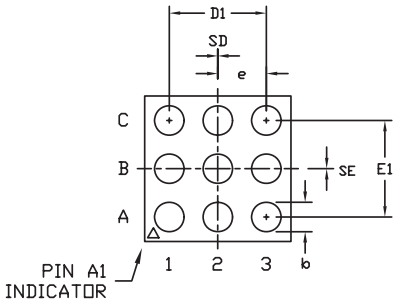


TOP VIEW

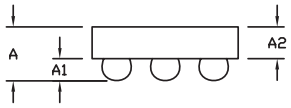
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.00 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.00 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B9-1	1.52±0.05	1.52±0.05	NONE
B9-2	1.52±0.05	1.52±0.05	B2
B9-3	1.52±0.05	1.52±0.05	B1, B2, B3
B9-4	1.60±0.05	1.60±0.05	NONE
B9-5	1.60±0.05	1.60±0.05	B2
B9-6	1.60±0.05	1.60±0.05	B1, B2, B3
B9-7	1.52±0.05	1.52±0.05	A2, B1, B2, B3, C2
B9-8	1.98±0.05	1.75±0.05	B1, B2, B3

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



BOTTOM VIEW



SIDE VIEW

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 3x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0093	L	1/1

Low IBIAS, +1.4V/800nA, Rail-to-Rail Op Amps with +1.2V Buffered Reference

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
5	11/09	Updated TOC 20	7

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